



RN-8087

B. E. - II (Sem. III) (Electrical) Examination
May / June - 2010
Analog & Digital Electronics
(New Course)

Time : 3 Hours]

[Total Marks :

Instructions :

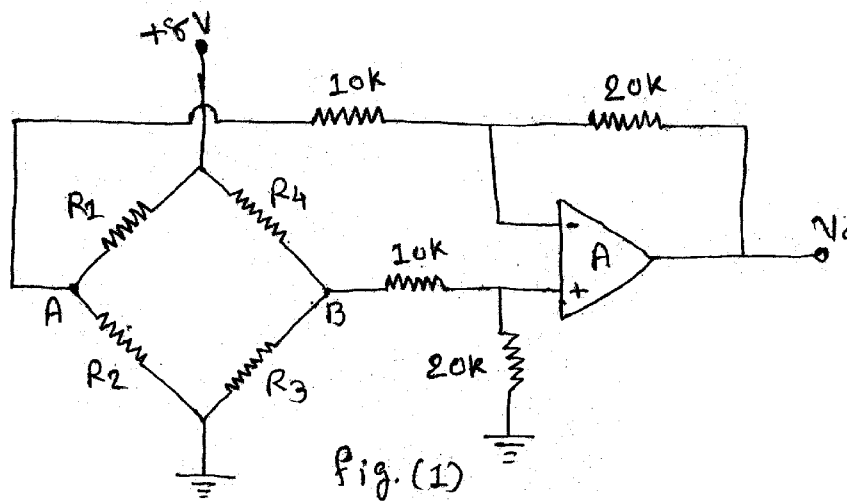
(1)

नीचे दशांशविकल्प निशान्चीवाणी विगतो उत्तरवडी पर अवश्य वजवी. Fillup strictly the details of signs on your answer book.	Seat No. :
Name of the Examination :	<input type="text"/>
B. E. - 2 (Sem. 3) (Electrical)	<input type="text"/>
Name of the Subject :	<input type="text"/>
Analog & Digital Electronics	<input type="text"/>
Subject Code No. : <input type="text" value="8"/> <input type="text" value="0"/> <input type="text" value="8"/> <input type="text" value="7"/>	<input type="text"/>
Section No. (1, 2,.....) : <input type="text" value="1&2"/>	
Student's Signature	

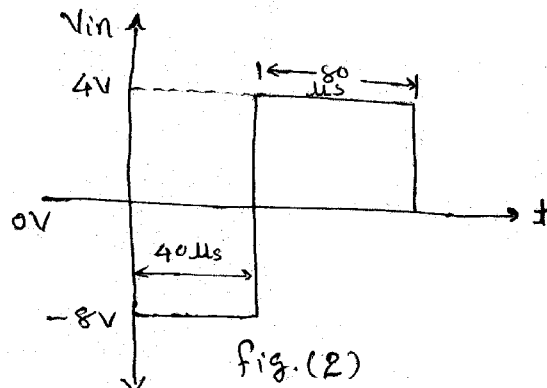
- (2) All abbreviations and symbols have their usual meanings.
- (3) Missing data may be assumed wherever necessary.
- (4) Figures on the **right** indicate full marks to that part.
- (5) Answer to the two sections must be written in **separate** answer books.

SECTION - I

- 1 (a) Answer the following questions : 10
- (i) Draw the schematic of inverting comparator with input and output waveforms (a) If V_{ref} is positive (b) If V_{ref} is negative.
 - (ii) Define a filter. How filters are classified?
 - (iii) What is a multivibrator circuit? What is its use? State its types.
 - (iv) Draw the frequencyt transistor circuit using PLL.
 - (v) Draw the block diagram of VFC32.
- (b) Find the output voltage. When (a) $R_1=R_2=R_3=R_4 = 2 \text{ k } \Omega$ and (b) $R_1 = R_2 = R_3 = 2 \text{ k } \Omega$ and $R_4 = 2.2 \text{ k } \Omega$. Assume ideal op-amp and the impedance at node A and node B do not load the preceding bridge circuit.



- (c) Define the following terms of D/A converter : 4
- (i) Resolution
 - (ii) Monotonicity
 - (iii) Conversion time
 - (iv) Linearity.
- 2 (a) Explain in detail requirements of a good instrumentation amplifier. 4
- (b) The practical integrator circuit has $R_1 = 10 \text{ k } \Omega$, 6
 $R_F = 1 \text{ m } \Omega$, $C_F = 5 \text{ nF}$. Sketch the output for the i/p shown in Fig. 2.



- (c) For the circuit shown in Fig. 3 determine the output voltage V_o . 4

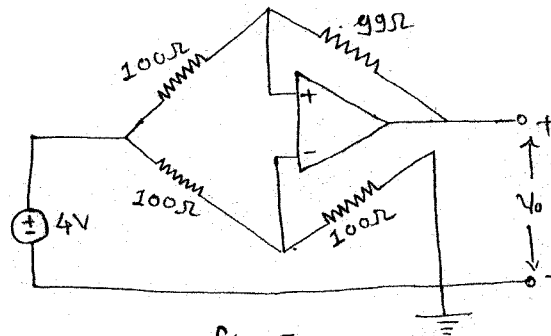


Fig. 3

OR

(c) Draw and explain the basic CMOS inverter circuit. 4

3 Attempt any **three** out of four. 18

- (i) For the circuit of Fig. 4 show that $V_o = G_1V_1 + G_2V_2 + G_3V_3$ and find the values of G_1 , G_2 and G_3 . Also find the values of V_o if (a) R_4 is short circuited (b) R_4 is removed (c) R_1 is short circuited.

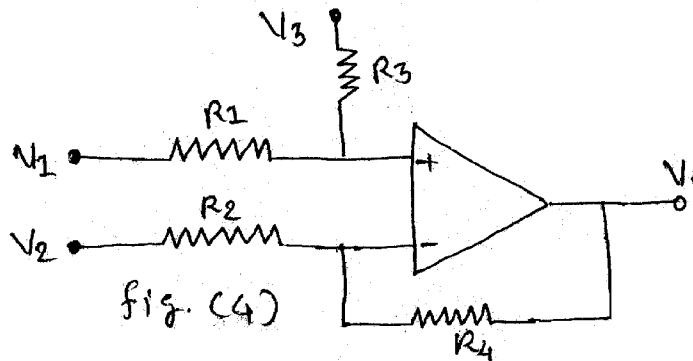


Fig. (4)

- (ii) Draw and explain the operation of astable multivibrator using op-amp.
 (iii) Explain the working of op-amp inverting amplifier. Drive the expression for its voltage gain.
 (iv) Find V_o for the circuit in Fig. 5.

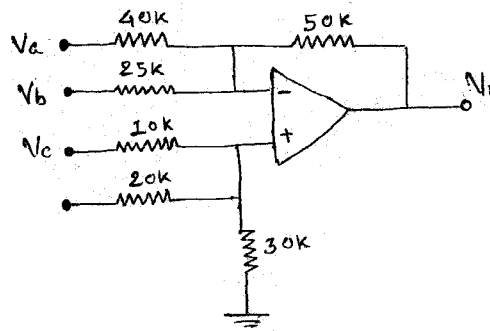


Fig. 5

SECTION - II

- 1 Attempt the following : 20**
- (a) (i) Convert : 10
- (a) $(1011.01)_2 = (\quad)_{10}$
- (b) $(204)_{10} = (\quad)_8$
- (ii) Prove : $(A + \bar{B} + A\bar{B})(A + B)(\bar{A}B) = 0$
- Simplify : $A\bar{B} + \bar{A}B + AB + \bar{A}\bar{B}$
- (iii) Draw the circuit using NAND gate and NOR gate.
- $F = AB + CD$
- (iv) Simplify and draw the logic diagram using K'map
- $F = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D + \bar{A}BCD + ABCD + A\bar{B}\bar{C}D + ABCD$
- (v) Draw half adder circuit using its truth table.
- (b) Prove that : full adder circuit can be implemented 5
using two half adder circuit. Using circuit and expression.
- (c) Implement the following multiple o/p function using a suitable decoder.
- $F_1(A, B, C) = \sum m(1,5,6)$
- $F_2(A, B, C) = \sum (0,2,4,6)$
- 2 Attempt any two : 10**
- (i) Design (32×1) multiplexer circuit using four (8×1) multiplexer and one (2×4) decoder.
- (ii) Implement a full adder circuit using demultiplexer.
- (iii) Simplify the following expression once by considering the don't care condition and once by ignoring the don't care condition.
- $F = \sum m(1,4,8,12,13,15) + d(3,14)$
- 3 Attempt any two : 10**
- (i) Write
- (a) Comparison between counters and register.
- (b) Explain : Positive edge triggered D flip flop.
- (c) Explain : Bidirectional shift register.